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10/796,416	03/10/2004	Gerald Harron	85195-502 ADB	9044

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ADE & COMPANY INC.
2157 Henderson Highway
WINNIPEG, MB R2G1P9
CANADA

EXAMINER
TORRES, JUAN A

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/796,416	HARRON ET AL.
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,6-18 and 20-33* is/are rejected.

7)☒ Claim(s) *2,4,5 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/25/2004*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 06/25/2004 is in

compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure

statement is being considered by the examiner.

Drawings

The drawings are objected to because:

a) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5)

because they include the following reference character(s) not mentioned in the

description: "41" and "42" (in figure 4; the reference to 41 in page 7 line 9 is incorrect

[see specification objections]); "112", "104a", "104b", "105a", and "105b" (in figure 2);

b) The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5)

because they do not include the following reference sign(s) mentioned in the

description: "102"; "106"; "111" (see page 8 lines 7, 8, 16 and 19; page 10 line 21);

"101a" and "101b" (see page 9 lines 11-12) "105 (page 10 lines 8, 9 and 10)' "106"

(page 10 line 14); "104" and "108 (see page 11 lines 1, 2, 10, 11, 16); "102, "105", "106",

108", "104" (page 12 lines 7, 8, 9, 15 and 16); "109 (page 13 line 11); "104' "102 and

105" (page 14 lines 4 and 12); "102", "105 in page 15 lines 15, 16 and 22; and "106"

(page 16 line 1); and

c) In table 1 lines 1 and 2 the recitation "Mhz" is improper (see table 1 lines 3 and

5); it is suggested to be changed to "MHz".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The

disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because exceed 150 words in length. Correction is required. See MPEP § 608.01(b).

The first paragraph of 35 U.S.C. 112 indicates that "The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such <u>full, clear, concise, and exact terms</u> as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention"

The disclosure is objected to because of the following informalities:

a) The recitation in page 1 lines 9-13 "This application is related to applications filed on the same day by the same inventors under Attorney Docket 85195-602 ADB entitled APPARATUS FOR FRACTIONAL RF SIGNAL SYNTHESIS WITH PHASE MODULATION and Attorney Docket 85195-402 ADB entitled APPARATUS FOR FRACTIONAL RF SIGNAL SYNTHESIS the disclosures of which are incorporated herein by reference" is improper because the cited applications should be referenced by the Serial number; it is suggested to indicate the Application Serial numbers (the first one seems to be 10/796,415, and the second one may be 10/796,417 [in this case the title seems to be different, "METHOD AND APPARATUS FOR FRACTIONAL RF SIGNAL SYNTHESIS", <u>the Applicant is requested to double check the appropriate title</u>])

b) The recitation "$2^{\wedge n}$" (at least in page 3 lines 9 and 13; page 8 line 20; page 10 line 6; page 11 line 23; page 12 line 2 is improper (see page 3 line 2); it is suggested to be changed to "2^n";

c) The recitation "sin x/x" in page 3 line 21, page 13 lines 13, 14 and 22 is improper; it is suggested to be changed to "(sin x)/x";

d) The recitation "$((y_r(nT')))$" in page 7 line 5 is improper because it is not properly constructed; it is suggested to be changed to "$(y_r(nT'))$";

e) The recitation "41" in page 7 line 9 is improper (see figure 1); it is suggested to be changed to "40";

f) The recitation "$((y_r(nT')))$" in page 3 lines 9 and 13 is improper because it is not properly constructed; it is suggested to be changed to ""$(y_r(nT'))$";

g) The recitation "$2^{\wedge 12}$" in page 10 line 16 is improper; it is suggested to be changed to "2^{12}";

h) The recitation "244 KHz" in page 12 line 2 is improper, because thousands is indicated with lower case k; it is suggested to be changed to "244 kHz"; and

i) The recitation "15.2 KHz" in page 12 line 5 is improper, because thousands is indicated with lower case k; it is suggested to be changed to "15.2 kHz";

Appropriate correction is required.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 4, 5, 14, 16, 20, 21 and 27 are objected to because of the following informalities:

Regarding claim 4, the recitation in line 3 of claim 4 "2n" is improper (see specification objections above; see also PGPUB of the present application page 5 left column last line); it is suggested to be changed to "2^n".

Regarding claim 5, the recitation in line 5 of claim 5 "$2^{^n}$" is improper (see specification objections above; see also PGPUB of the present application page 5 right column); it is suggested to be changed to "2^n".

Regarding claim 14, the recitation in line 2 of claim 14 "sin x/x" is improper (see specification objections above); it is suggested to be changed to "(sin x)/x".

Regarding claim 16, the recitation in line 1 of claim 16 "wherein an there are" is improper because is not properly constructed; it is suggested to be changed to "wherein there are".

Regarding claim 20, the recitation in line 3 of claim 20 "2^n" is improper (see specification objections above); it is suggested to be changed to "2^n".

Regarding per claim 21, claim 21 is objected because it depends directly from claim 20 and claim 20 is objected.

Regarding claim 27, the recitation in line 3 of claim 27 "$2^{^n}$" is improper (see specification objections above; see also PGPUB of the present application page 6 right column); it is suggested to be changed to "2^n".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8, 26 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 8, claim 8 recites the limitation "said reference edge " in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 26, claim 26 is rejected because depends directly from claim 8 and claim 8 is rejected.

Regarding claim 26, claim 26 recites the limitation "said increment values" in lines 1-2. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 31, claim 31 recites the limitation " wherein all the answers of the pattern are precomputed and stored " in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 6-10, 26, and 32-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Dress (US20020097790).

Regarding claim 1, Dress discloses a high speed reference clock providing in an input signal having a series of pulses at a frequency of the reference clock which is higher than the desired output frequency (figure 10 block 1001; paragraph [0063]; and figure 13 block 1310 paragraph [0070]); two programmable digital delay elements each arranged to receive the reference pulses of the input reference clock and to generate therefrom using input data a respective one of two digital vectors (figure 10 block 1005; paragraph [0063]); and a signal combining element for receiving the digital vectors from the programmable digital delay elements and for generating the QAM RF signal therefrom (figure 10 block 1009; paragraph [0065]).

Regarding claim 6, Dress discloses claim 1, Dress also discloses that the reference clock is an external input with high frequency absolute accuracy and very low phase noise performance (paragraph [0063]).

Regarding claim 7, Dress discloses claim 1, Dress also discloses that the delay elements delay a reference edge of the input reference clock (paragraph [0063]).

Regarding claim 8, Dress discloses claim 7, Dress also discloses that the reference edge may be either the rising or falling edge of the reference clock (paragraph [0063], inherently a clock has rising and falling edges).

Regarding claim 9, Dress discloses claim 1, Dress also discloses that the delay elements have separate controls for producing the rising and falling edges of the output from the same input edge of the reference clock (paragraph [0063]).

Regarding claim 10, Dress discloses claim 1, Dress also discloses that the implementation of the delay elements may vary by altering the input clock signal (paragraph [0063]).

Regarding claim 26, Dress discloses claim 8, Dress also discloses that the increment values for the rising and falling edges are the same value (paragraph [0063], inherently a clock has rising and falling edges).

Regarding claim 32, Dress discloses claim 1, Dress also discloses that the components are formed fully digitally in an ASIC with no requirement for a voltage controlled oscillator, loop filter, or Digital to Analog converter (figure 13, paragraph [0070]).

Regarding claim 33, Dress discloses claim 1, Dress also discloses amplification and filtering of the output to produce a signal that is higher in amplitude and/or having less harmonics (figure 13 blocks 1360 and 1370, paragraph [0070]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 11, 12, 20-24 and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dress as applied to claim 1 above, and further in view of Wolaver (US 5627500 A).

Regarding claim 3, Dress discloses claim 1, Dress doesn't disclose that the programmable digital delay elements comprise high speed adders/accumulators where the adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference signal. Wolaver discloses a programmable digital delay elements comprise high speed adders/accumulators where the adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference signal (figure 2 block 20 and 22 column 1 lines 32-46). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the accumulator and adder disclosed by Wolaver. The suggestion/motivation for doing so would have been to use a known technique to delay a signal (Wolaver column 1 lines 32-46).

Regarding claim 11, Dress and Wolaver disclose claim 3, Wolaver also discloses that the adders/accumulators are arranged to determine the amount of delay implemented by the delay elements on the reference edge to produce the desired RF frequency (figure 2 block 20 and 22 column 1 lines 32-46). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the accumulator and adder disclosed by Wolaver. The suggestion/motivation for doing so

would have been to use a known technique to delay a signal (Wolaver column 1 lines 32-46).

Regarding claim 12, Dress discloses claim 1, Dress doesn't disclose modulation adders which add in the positive or negative phase offset to the accumulator value to produce the required modulation. Wolaver discloses modulation adders which add in the positive or negative phase offset to the accumulator value to produce the required modulation (figure 2 block 20 and 22 column 1 lines 32-46). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the accumulator and adder disclosed by Wolaver. The suggestion/motivation for doing so would have been to use a known technique to delay a signal (Wolaver column 1 lines 32-46).

Regarding claim 20, Dress discloses claim 1, Dress doesn't disclose programmable digital delay elements are arranged such that 360 degrees of phase delay of the programmable delay is calibrated to 2^n of the phase accumulator value using a look up table or microprocessor. Wolaver discloses programmable digital delay elements are arranged such that 360 degrees of phase delay of the programmable delay is calibrated to 2^n of the phase accumulator value using a look up table or microprocessor (figure 2 block 24 column 1 lines 32-46 and figures 10 and 15 block 78 column 7 line 30 to column 8 line 6). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the

invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the look up table technique disclosed by Wolaver. The suggestion/motivation for doing so would have been to use a known technique to delay a signal (Wolaver column 1 lines 32-46).

Regarding claim 21, Dress and Wolaver disclose claim 20, Wolaver also discloses that the lookup table has a multiple set of lookup tables to be used for temperature compensation of the programmable delay element (figure 2 block 20 and 22 column 1 lines 32-46 and column 10 line 66 to column 11 line 7). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the accumulator and adder disclosed by Wolaver. The suggestion/motivation for doing so would have been to use a known technique to delay a signal (Wolaver column 1 lines 32-46).

Regarding claim 22, Dress discloses claim 1, Dress doesn't disclose flipflops which are used to combine the separate rising and falling edge delays to form any desired duty cycle output. Wolaver discloses flipflops which are used to combine the separate rising and falling edge delays to form any desired duty cycle output (figure 14 block 88 column 8 lines 38-56). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the combiner technique disclosed by Wolaver.

The suggestion/motivation for doing so would have been to use a known technique to

multiplex the delay lines (Wolaver column 8 lines 41-45).

Regarding claim 23, Dress and Wolaver disclose claim 22, Wolaver also

discloses that the programmable digital delay elements are arranged such that the duty

cycle of the output is varied by changing the difference in the initialization values of the

accumulators for the rising and falling edge delay control (figure 2 block 20 and 22

column 1 lines 32-46 and column 10 line 66 to column 11 line 7). Dress and Wolaver

are analogous art because they are from the same field of endeavor of Digital

Communications. At the time of the invention, it would have been obvious to a person of

ordinary skill in the art to incorporate in the transmission system disclosed by Dress the

accumulator and adder disclosed by Wolaver. The suggestion/motivation for doing so

would have been to use a known technique to delay a signal (Wolaver column 1 lines

32-46).

Regarding claim 24, Dress and Wolaver disclose claim 22, Wolaver also

discloses that the programmable digital delay elements are arranged such that the

output duty cycle is not dependent on the input duty cycle (figure 12 and 13 column 8

lines 16-29). Dress and Wolaver are analogous art because they are from the same

field of endeavor of Digital Communications. At the time of the invention, it would have

been obvious to a person of ordinary skill in the art to incorporate in the transmission

system disclosed by Dress the accumulator and adder disclosed by Wolaver. The

suggestion/motivation for doing so would have been to allow greater range (Wolaver

column 8 lines 16-19).

Regarding claim 28, Dress and Wolaver disclose claim 3, Wolaver also discloses that increasing the number of bits in the adder math increases the frequency resolution with negligible degradation in the phase noise performance (figure 12 and 13 column 7 lines 34-43). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the accumulator and adder disclosed by Wolaver. The suggestion/motivation for doing so would have been to obtain fine resolution (Wolaver column 7 lines 34-43).

Regarding claim 29, Dress and Wolaver disclose claim 3, Wolaver also discloses that the number of bits of math used in the adder can be equal to or exceed the number of bits of control in lookup table and/or the programmable delay (figure 12 and 13 column 7 lines 34-43). Dress and Wolaver are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the accumulator and adder disclosed by Wolaver. The suggestion/motivation for doing so would have been to obtain fine resolution (Wolaver column 7 lines 34-43).

Regarding claim 30, Dress and Wolaver disclose claim 3, Dress also discloses parallel processing increase the speed (figure 10 block 1004 paragraph [0062]).

Regarding claim 31, Dress and Wolaver disclose claim 3, Wolaver also discloses that the programmable digital delay elements are arranged such that the

adders/accumulators can be implemented in a larger lookup table where all the answers

of the pattern are precomputed and stored (figure 12 and 13 column 7 lines 34-43).

Dress and Wolaver are analogous art because they are from the same field of endeavor

of Digital Communications. At the time of the invention, it would have been obvious to a

person of ordinary skill in the art to incorporate in the transmission system disclosed by

Dress the accumulator and adder disclosed by Wolaver. The suggestion/motivation for

doing so would have been to obtain fine resolution (Wolaver column 7 lines 34-43).

Claims 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Dress as applied to claim 1 above, and further in view of Norsworthy (US

20040037363 A1).

Regarding claim 13, Dress discloses claim 1, Dress doesn't disclose an

interpolator which interpolates the input data in the form of base band modulated

information. Norsworthy discloses an interpolator which interpolates the input data in the

form of base band modulated information (figure 3 block 318 paragraph [0074]). Dress

and Norsworthy are analogous art because they are from the same field of endeavor of

Digital Communications. At the time of the invention, it would have been obvious to a

person of ordinary skill in the art to incorporate in the transmission system disclosed by

Dress the interpolator disclosed by Norsworthy. The suggestion/motivation for doing so

would have been to reduce the quantization noise (Norsworthy paragraph [0074]).

Regarding claim 14, Dress and Norsworthy disclose claim 13, Norsworthy also

discloses that interpolator is a linear interpolator or a sin x/x interpolator filter (figure 3

block 318 paragraph [0086]). Dress and Norsworthy are analogous art because they are

from the same field of endeavor of Digital Communications. At the time of the invention,
it would have been obvious to a person of ordinary skill in the art to incorporate in the
transmission system disclosed by Dress the interpolator disclosed by Norsworthy. The
suggestion/motivation for doing so would have been to reduce the quantization noise
(Norsworthy paragraph [0074]).

Regarding claim 16, Dress discloses claim 1, Dress doesn't disclose separate
interpolators for both the rising and falling pulse edges. Norsworthy discloses separate
interpolators for both the rising and falling pulse edges (figure 3 block 312 and 318
paragraph [0060]-[0061] and [0074]-[0075]). Dress and Norsworthy are analogous art
because they are from the same field of endeavor of Digital Communications. At the
time of the invention, it would have been obvious to a person of ordinary skill in the art
to incorporate in the transmission system disclosed by Dress the interpolator disclosed
by Norsworthy. The suggestion/motivation for doing so would have been to reduce the
quantization noise (Norsworthy paragraph [0074]).

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable
over Dress as applied to claim 1 above, and further in view of Nakagawa (US 5714896
A).

Regarding claim 17, Dress discloses claim 1, Dress doesn't disclose a pulse
swallow circuit which is arranged to ignore/block multiple reference clock pulses.
Nakagawa discloses a pulse swallow circuit which is arranged to ignore/block multiple
reference clock pulses (figure 8 column 2 lines 13-53). Dress and Nakagawa are
analogous art because they are from the same field of endeavor of Digital

Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the pulse swallow circuit disclosed by Nakagawa. The suggestion/motivation for doing so would have been to change the frequency of the frequency synthesizer (Nakagawa column 1 lines 6-11 and column 2 lines 51-53).

Regarding claim 18, Dress and Nakagawa disclose claim 17, Nakagawa also discloses that the pulse swallow circuit is arranged such that it controlled by the carry bits in order to extend the delay to multi cycles of the input reference clock (figure 8 column 2 lines 13-53). Dress and Nakagawa are analogous art because they are from the same field of endeavor of Digital Communications. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the transmission system disclosed by Dress the pulse swallow circuit disclosed by Nakagawa. The suggestion/motivation for doing so would have been to change the frequency of the frequency synthesizer (Nakagawa column 1 lines 6-11 and column 2 lines 51-53).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dress and Norsworthy as applied to claim 13 above, and further in view of Berangi (US 20050163248 A1).

Regarding claim 15, Dress and Norsworthy disclose claim 13, Dress and Norsworthy don't specifically disclose that the interpolator effects interpolation up to the reference clock rate so as to avoid use of a reconstruction filter. Berangi discloses the interpolator effects interpolation up to the reference clock rate so as to avoid use of a

reconstruction filter (figure 3 block 318 paragraph [0074]). Dress, Norsworthy and

Berangi are analogous art because they are from the same field of endeavor of Digital

Communications. At the time of the invention, it would have been obvious to a person of

ordinary skill in the art to incorporate in the transmission system disclosed by Dress and

Norsworthy the interpolator disclosed by Berangi. The suggestion/motivation for doing

so would have been to reduce the requirements on the reconstruction filter (Berangi

paragraph [0087]).

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dress

and Wolaver as applied to claim 22 above, and further in view of Park (US 6373902

B1).

Regarding claim 25, Dress and Wolaver disclose claim 13, Dress and Wolaver

don't specifically disclose that the two phase modulated vector outputs of the flipflops is

amplified using nonlinear amplifiers. Park discloses the two phase modulated vector

outputs are amplified using nonlinear amplifiers (figure 2 block 223 column 6 lines 10-

14). Dress, Wolaver and Park are analogous art because they are from the same field

of endeavor of Digital Communications. At the time of the invention, it would have been

obvious to a person of ordinary skill in the art to incorporate in the transmission system

disclosed by Dress and Wolaver the amplifier disclosed by Park. The

suggestion/motivation for doing so would have been to amplify the transmission signal

(Park column 6 lines 10-14).

Allowable Subject Matter

Claims 2, 4, 5 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

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Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
6-25-2007